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EXAMINER
PATEL, GAUTAM

ART UNIT	PAPER NUMBER
2655	14

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Please find below and/or attached an Office communication concerning this application or proceeding.

TS

Office Action Summary	Application No.	Applicant(s)	
	09/338,473	KIM ET AL.	
	Examiner	Art Unit	
	Gautam R. Patel	2655	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 June 2003*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *9-25* is/are allowed.

6)☒ Claim(s) *1-8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. Claims 1-25 are pending for the examination.

CPA STATUS

2. The request filed on 6-30-03 for a Continued Prosecution Application (CPA) under 37 CFR 1.53(d) based on parent Application No. 09/338,473 is acceptable and a CPA has been established. An action on the CPA follows.

Claim Rejections - 35 U.S.C. § 103

3. The following is a quotation of 35 U.S.C. § 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

4. Claims 1-8 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Kai et al., US. patent 5,287,309 (hereafter Kai) in view of Koppala (US. patent 6,67,488) (hereafter Koppala).

As to claim 1, Kai discloses the invention as claimed [see Figs. 1-5] including a stack storage, a stack pointer circuit and a control signal comprising:

a stack storage [fig. 2, unit 5] comprising a plurality of banks [fig. 2, units 10 and 11] each comprising storage locations [col. 4, lines 14-20 and 27-39];

a stack pointer circuit [fig. 2, units 6, 7 and 8] comprising a bank pointer for each bank [{(SP_M + SP_L), SP_L} for first bank; and {SP_M, SP_L}, for second bank] wherein each bank pointer points to a storage location of a corresponding bank, and wherein the stack pointer circuit is responsive to at least one control signal [fig. 2, output of unit 7][col. 5, lines 45-62] [col. 4, line 58 to col. 5, line 16];

Kai disclose all of the above elements. Kai also discloses that a single pointer [SPM] can perform two operations simultaneously [PUSH and POP], and one signal is for pushing [or inserting] a word on the stack. Kai does not disclose that this single pointer can also POP [remove] two-word item form the stack, but Kai suggest that variation of the simultaneous POP and PUSH can be implemented, and this can be done by determination of the even and odd addresses and simple mathematical transformation [col. 2, lines 18-28; Kai]. Also Koppala clearly discloses that control signal can be used for inserting a two-word or multi-word item into said stack storage and removing a two-word item from adjacent locations at a given time [col. 24, lines 21-40]. Both Kai and Koppala discloses systems with PUSH and POP operation, both discloses stack structure and several pointers.

One of ordinary skill in the art would have realized that faster circuit operation is a desired function to have, and performing two operations with a single command makes system faster, and also it is possible to execute two POP operation [or removing two-word item form the stack] instead of one PUSH and one POP operation in the system of Kai by simply transforming the logic as suggested by Kai.

Also Koppala clearly discloses that "The most common stack manipulation for stack based computing system is to pop the two words from a stack and to push a data word onto the top of the stack" [col. 24, lines 29-32]. Therefore, it would have been obvious to one of ordinary skill in the art at the time invention to have provided, capability to remove two-word item from the stack storage, to the circuit of Kai with as taught and suggested by Koppala, because it would have provided to a mechanism to execute the either two PUSH or two POP operation on the stack, thus making the stack operation much faster.

NOTE: Two separate banks [fig. 2, units 10 and 11] and each bank pointers going to them causes multi-word pop or push operation in a combined system

5. As to claim 2, Kai discloses:

a stack storage [fig. 2, unit 5] comprising a plurality of banks [fig. 2, bank 10 and bank 11] each comprising storage locations for storing stack items [col. 4, lines 14-20 and 27-39];

a plurality of stack pointers [SP_M and SP_L; see fig. 2, output of unit 6], the stack pointers comprising a main stack pointer [fig. 2, output of unit 6] for pointing to a top location of the stack storage and a bank pointer for each bank [{(SP_M + SP_L), SP_L} for first bank; and {SP_M, SP_L}, for second bank], wherein each bank pointer points to a storage location of a corresponding bank based on the content of the main stack pointer [fig. 2, unit 6] [col. 4, lines 58-63]; and

a controller [fig. 2, units 7, 8 and 9] responsive to at least one of the decoding signals for inserting bank address data into at least two bank pointers to perform multi-word push or multi-word pop operation [col. 4, lines 21-63];

NOTE: Two separate banks [fig. 2, units 10 and 11] and each bank pointers going to them causes multi-word pop or push operation in a combined system

6. As to claim 3, Kai discloses:

each location of said stack storage is configured for storing a one-word item [inherently one-word is stored in stack memory].

7. As to claim 4, Kai discloses:

a two word item is one of inserted into and removed from two adjacent locations at a given time [col. 24, lines 21-40].

8. As to claim 5, Koppala discloses:

said stack storage control circuit increases and decreases the content of said stack pointer by one when the decoding signals indicate a one-word stack operation;

and wherein said stack storage control circuit increases and decreases the content of said stack pointer by two when the decoding signals indicate a two-word stack operation [col. 24, lines 21-61].

9. As to claim 6, Kai discloses:

a stack storage [fig. 2, unit 5] including a plurality of locations, wherein each of the locations of said stack storage is assigned to one of a first [fig. 2, unit 10] and a second bank [fig. 2, unit 11] [col. 4, lines 27-39];

a main stack pointer [fig. 2, unit 6, SPM] for pointing to a location of said stack storage [col. 4, lines 59-63];

a first bank stack pointer [fig. 2, unit SPL] for pointing to a location assigned to said first bank [fig. 2, unit 10] [col. 5, lines 17-62];

a second bank stack pointer [fig. 2, unit SPL bar] for pointing to a location assigned to said second bank [fig. 2, unit 11] [col. 5, lines 17-62];

an instruction decoder [inherently present] for decoding a stack-based instruction and generating a plurality of decoding signals [col. 4, lines 14-20]; and

a stack pointer control logic circuit [fig. 2, units 7, 8 and 9] for controlling said first and second bank stack pointers in response to at least one of the decoding signals to insert bank address data into the first and second bank stack pointers based on the content of the main stack pointer to perform a multi-word push or multi-word pop operation [col. 4, lines 21-63];

10. As to claim 7 Kai discloses:

said stack storage comprises 2 n+1 locations, n being a positive integer, and wherein the first bank and the second bank each include 2 n locations [col. 4, lines 46-57].

11. As to claim 8 Kai discloses:

one of the first and second banks includes locations with addresses having a least significant bit of logic `0' and the other of the first and second banks includes locations with addresses having a least significant bit of logic `1' [col. 4, lines 40-45].

Kai and Koppala were cited as prior art references in paper no. 4, mailed 7-2-01.

12. Applicant's arguments filed on 10-01-01 (Paper # 5) have been fully considered but they are not deemed to be persuasive for the following reasons.

13. In the REMARKS, the Applicant argues as follows:

A) That: "To, establish a *prima facia* case of obviousness based on the combination of Kai and Koppala, various criteria must be met. For instance, the combination *must* [original emphasis] teach or suggest all of the claim limitations. Further, there must be some suggestion or motivation in the references or in the knowledge generally available to one skilled in the art to combine their teachings. The teachings or suggestion to make the claimed combination must both be found in the prior art and not based on the hindsight in view of the applicant's disclosure ...

Here, it is respectfully submitted that at very minimum the combination of Kai and Koppala is legally deficient to establish a prima facia case of obviousness against claims 1, 2 and 6, for at least following reasons: (1) there is no motivation to combine the teachings of Kai and Koppala to derive the claimed invention; and (2) even if Kai and Koppala are combined, such combination does not teach or suggest all the elements of claim 1, 2 and 6." [page 2, para. 3-4; REMARKS].

FIRST: As to all the limitations, careful examination of rejection of claims 1, 2 and 6 shows that ALL limitations are covered in detail including explanation [in form of NOTE] what the combination represents.

SECOND: As to motivation or teachings Kai very clearly teaches that there are many modifications equivalent to the embodiments...and These modifications are not specified here, however it should be understood that a great many systems derivatives

and equivalent to the embodiment can be derived by simple mathematical transformation ..." [col. 2. Lines 18-28; Kai].

THIRD: It should be pointed out that:

The test of the obviousness is:

"whether the teachings of the prior art, taken as a whole, would have made obvious the claimed invention,". As shown in *In re Gorman*, 933 F. 2d at 986, 18 USPQ2d at 1888.

Subject matter is unpatentable under section 103 if it "'would have been obvious .... to a person having ordinary skill in the art.' While there must be some teaching, reason, suggestion, or motivation to combine existing elements to produce the claimed device, **it is not necessary that the cited references or prior art specifically suggest making the combination.**" As shown in *In re Nilssen*, 851 F. 2d 1401, 1403, 7 USPQ2d 1500, 1502 (Fed. Cir. 1988).

Such suggestion or motivation to combine prior art teachings can derive solely from the existence of a teaching, which one of ordinary skill in the art would be presumed to know, and the use of that teaching to solve the same [or] similar problem which it addresses." As shown in *In re wood*, 599 F. 2d 1032, 1037, 202 USPQ 171, 174 (CCPA 1979).

"In sum, it is off the mark for litigants to argue, as many do, that an invention cannot be held to have been obvious unless a suggestion to combine prior art teachings is found *in* a specific reference." As shown in *In re Oetiker*, 24 USPQ2d 1443 (CAFC 1992).

Accordingly, Kai or Koppala are not required to disclose or specifically suggest particular elements. Instead the measure is what the teachings of Kai or Koppala would suggest to one of ordinary skill in the art, not what 1 or Koppala specifically suggests.

B) That: "the structures and functions of the stack circuits of Kai and Koppala are so fundamentally different [original emphasis] from those of the claimed inventions, that one of ordinary skill in the art would not be motivated combine the teachings of Kai and Koppala to derive the claimed inventions." [page 2, para. 5; REMARKS].

FIRST: Structure of Kai and Koppala are very similar as pointed out in the rejection of claims above. And therefore there combination is very proper because both Kai and Koppala discloses systems with PUSH and POP operation, both discloses stack structure, which is central to the invention, and several pointers.

SECOND; As to how Kai and Koppala structure different from what is being **claimed** has not been pointed out by the Applicants. Examiners stands by his rejection and reason for rejection.

C) That: "In general, Kai is directed to a stack memory framework capable of simultaneously executing *Push* (write) and *Pop* (read) operations, with respect to an address in a Stack Pointer. The Kai framework enables both Push and Pop operations to be simultaneously performed ... using the Kai framework, a Last-in-First-Out (LIFO) stack may store invalid data [original emphasis] in stack ...[page 3, para. 2; REMARKS].

FIRST: Kai disclose BOTH operation FIFO and LIFO. One bank works on FIFO and second bank works on LIFO.

SECOND: It should be pointed out 103 rejection was used NOT 102. The Examiner well aware that Kai does not teach FIFO operation of on both stacks. That aspect is taught by Koppala and Koppala is used for that limitation not Kai.

THIRD: To put it in simple words, Kai discloses simultaneous POP and PUSH operation, not PUSH-PUSH or a POP-POP. That is two simultaneous either PUSH operations or POP operations. However these simultaneous operations either PUSH or POP are clearly disclosed by Koppala.

D) That: "Therefore, although Kai discloses a two-bank stack memory ...to provide high-speed processing." [page 5, para. 2; REMARKS].

FIRST: For multi-word pop or multi-word push operation, Koppala was used NOT Kai.

SECOND: As to this argument, please see detailed explanation in paragraph 13, section C), supra.

E) That: "Koppala does not cure the deficiencies of Kai in this regard. Although Koppala arguably discloses performing multi-word stack operations, Koppala implements a *multi-port memory device* [original emphasis] to preform multiple read and/or write operations using different ports.....Koppala does not disclose or suggest a multi-bank framework for reading or writing multi-word data." [page 5, para. 3; REMARKS].

FIRST: The Applicants are correct that Koppala does clearly teach multi-word stack operations. It should be pointed out again, that this is 103 rejection NOT 102, therefore Koppala does not teach ALL limitations.

SECOND: What else Koppala teaches or does not teach besides multi-word stack operations is irrelevant to the arguments, since the Applicants are claiming "a hardware stack, comprising:".

F) That: "Examiner essentially contends ...one of ordinary skill in the art would not be motivated to combine the teachings." [page 6, para. 1 to page 7, para. 1; REMARKS].

Please see paragraph 13, sections A) to E), supra.

G) That: combination does not disclose or suggest a circuit having *a bank pointer associated with each bank of a stack, wherein each bank pointer stores address data for its respective bank*, [original emphasis] as essentially claimed in claim 1, 2 and 6. In contrast, Kai discloses only a single stack pointer (6) (see Fig. 2) that stores an address over all of the stack memory (see, Col. 4, lines 68-60). The stack pointer (6) does not comprise a plurality of bank pointers that store the bank addresses [original emphasis]...as claimed." [page 7, para. 3; REMARKS].

FIRST: Kai discloses: *a bank pointer associated with each bank* [fig. 2, bank 10 and bank 11] *of a stack* [fig. 2, unit 5 and col. 4, line 21] [first bank pointer {(SP_M + SP_L), SP_L} for first bank [bank 10]; and a second bank pointer {SP_M, SP_L}, for second bank

[unit 11] *wherein each bank pointer stores address data for its respective bank* [col. 2, lines 3-17; Kai].

SECOND: The stack pointer does clearly comprise the two stack pointers [see fig. 2]. Notice output of 6 directly going to BOTH banks AND output of unit 8 also point to BOTH banks.

THIRD: Close inspection shows that unit 6 has TWO stack pointers SP_M and SP_L [fig. 2].

Allowable Subject Matter

14. Claims 9-25 are allowed over the prior art of record.

Claims 9 and 17 are allowable over the prior art of record since the cited references taken individually or in combination fails to particularly disclose a digital data processor which includes a stack pointer control logic circuit which includes "a first and second control logic for generating first and second control signal in response to the low-order bit portion of the output from the first selector and third and fourth selector respectively and a decoding signal from the instruction decoder and also second and third selector operating in response to first and second control signal". It is noted that the closest prior art, Kai and Koppala shows a similar apparatus which shows an adder and first selector. However Kai and Koppala fails to disclose a first and second control logic and second and third selector with all the detailed combinations.

15. All claims are drawn to the same invention claimed in the parent application prior to the filing of this Continued Prosecution Application under 37 CFR 1.53(d) and could have been finally rejected on the grounds and art of record in the next Office action. Accordingly, **THIS ACTION IS MADE FINAL** even though it is a first action after the filing under 37 CFR 1.53(d). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within

TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Contact information

16. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Gautam R. Patel whose telephone number is (703) 308-7940. The examiner can normally be reached on Monday through Thursday from 7:30 to 6.

The appropriate fax number for the organization (Group 2650) where this application or proceeding is assigned is (703) 872-9314.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ms. Doris To can be reached on (703) 305-4827.

Any inquiry of a general nature or relating to the status of this application should be directed to the group receptionist whose telephone number is (703) 305-4700 or the group Customer Service section whose telephone number is (703) 306-0377.

Gautam R. Patel
Patent Examiner
Group Art Unit 2655

December 9, 2003